

APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: AN AUTOMATIC GAIN CONTROL LOOP APPARATUS

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# AN AUTOMATIC GAIN CONTROL LOOP APPARATUS



## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to an automatic gain control loop, and more particularly, to an automatic gain control loop with a feedback loop.

### 2. Background of the Related Art

Presently, for radio frequency (RF) receivers, one of two different types of RF architectures, super-heterodyne and direct conversion are used for RF implementation. Generally direct conversion is considered to have the more straight forward approach. Unlike a super heterodyne receiver, a direct conversion receiver directly demodulates a desired signal to a base band signal, and does not need image filtering and Intermediate Frequency Surface Acoustic Wave (IF SAW) filtering. A low pass filter is typically used for channel selection, and thus the direct conversion receiver can be fully integrated. However, despite these architectural advantages, several practical problems, such as channel selection quality and direct current (DC) offsets have limited the availability of direct conversion receivers as commercial products.

Figure 1 is a general block diagram of a direct conversion receiver 1. An incoming analog RF signal is amplified at a first amplifier stage by a low noise amplifier (LNA) 10.

After this front-end amplification, the RF signal is demodulated into the base band signal by a mixer 20 that combines the RF signal with a local oscillation (LO) signal. The demodulated base band signal may be amplified by a post-mixer amplifier 30 and filtered by a channel selection filter 40, for eliminating out-of-band signals. The filtered base band signal is amplified by a second post filter amplifier 50, and is converted to a digital data stream by an analog-to-digital converter (ADC) 60.

Gain assignment and linearity are very important design factors for the direct conversion receiver 1, because channel selection is generally provided at a latter phase of the signal processing. Therefore, amplifiers, here shown as a post-mixer amplifier 30 and post-filter amplifier 50, are generally added to maximize the signal-to-noise ratio (SNR) and dynamic range before and after the channel selection filter 40.

An incoming RF has a time-varying magnitude in its amplitude, and needs gain control to maximize its dynamic range. This gain control should be provided prior to the channel selection filter 40. As shown in Fig. 1, the gain control is provided at the first amplifying stage by replacing the low noise amplifier LNA 10 with an automatic gain controller (AGC). However, since the input signal strength of an AGC can be very small, an input signal having a large input offset and path mismatch can corrupt the desired signal, and saturate the down stream stages.

For example, signal feedthrough leaks can occur at the low noise amplifier 10 input port and at the mixer 20 input port for the local oscillation signal, possibly from capacitor

and substrate coupling. This feedthrough (or LO leakage), is mixed with the LO signal, and produces DC offsets. A similar effect occurs when interference leaks from the inputs of the low noise amplifier 10 or the mixer 20, and is multiplied by itself. Further, low frequency device noises, such as  $1/f$  noise and transistor mismatches, contributes to DC offsets. The amount of the produced DC offset voltage can be greater than the input RF signal by more than several tens of dB. If this offset voltage is amplified by down stream gain stages, the amplified offset voltage can saturate the down stream circuits, prohibiting the amplification of the desired signal.

Accordingly, the related art direct conversion receiver 1 requires DC offset cancellation. The related art approach for DC offset cancellation uses a high-pass filtering of the DC offset voltage incorporated within the gain stages. The integration of the high-pass filtering depends on the corner frequency and the amount of DC offset rejection. Since the spectrum of DC offset is restricted around zero frequency, and the high-pass filtering must not impair the desired signal, the desired corner frequency should be as low as possible.

Figures 2a-2b show a related art DC offset cancelling circuit 100, having a single feedback loop 120, for providing high pass filtering of a DC offset. The DC offset cancelling circuit 100 includes a plurality of variable gain amplifiers (VGAs) 110 connected in series, and a DC offset cancelling loop 120 connected to an input port of the first VGA 110 and an output port of the last VGA 110. The DC offset cancelling loop

120 includes a DC offset cancelling circuit 130, which is a high pass filter. In Figures 2a and 2b, the incoming signal having a voltage  $V_{in}$  is amplified by the variable gain amplifiers (VGA #1, ... , VGA #N) to the level of an open-loop forward gain  $A_v$ , and is subjected to a gain of the DC offset cancelling loop  $A_{v,DC}$ , a DC offset gain  $G_m$ , and a capacitance  $C$  of the capacitor 180.

An overall transfer function is shown at Equation 1 as:

$$\frac{V_o}{V_{in}} = \frac{sA_v}{s + \frac{g_m A_v A_{v,DC}}{C}} \quad (1)$$

The AGC loop 100 has a corner frequency  $f_c$  shown at Equation 2 as:

$$f_c = \frac{g_m A_v A_{v,DC}}{2\pi C} \quad (2)$$

The capacitance  $C$  of the DC offset cancelling loop 120 increases as the corner frequency  $f_c$  decreases and the open loop forward gain  $A_v$  increases. The capacitance  $C$  value typically reaches several hundred of nF, and it is difficult to integrate a capacitor of this value on a single chip. Thus, the capacitor  $C$  is typically located at the outside of the chip. Unfortunately, when the off-chip capacitor is wired to the chip, a feedback connection is established, and some amount of noise is added via the bond wire coupling. This noise corrupts the signal integrity and degrades the signal-to-noise ratio (SNR).

For example, according to the above equation 1, the DC offset is reduced at a slope of 20 dB/decade from the corner frequency  $f_c$ . Rather than suppressing noise, this attenuation of DC offsets often amplifies noise at low frequency. For example, when the corner frequency  $f_c$  is 100KHz and the open loop forward gain  $A_v$  is 80dB, the offset signal at 100Hz is amplified by 20dB. Moreover, lowering the corner frequency  $f_c$  provides the undesirable effect of reducing the amount of DC offset rejection. Accordingly, related art AGC loops do not simultaneously provide low corner frequency with a high amount of DC offset rejection.

### SUMMARY OF THE INVENTION

An object of the invention is to at least substantially obviate the above problems and/or disadvantages of the related art, and to provide at least the advantages described hereinafter.

A further object of the present invention is to provide a DC offset cancelling apparatus.

Another object of the present invention is to simultaneously provide a lower corner frequency and high DC offset voltage rejection.

Still another object of the present invention is to provide a single chip bypass filter.

Yet another object of the present invention is to decrease a total capacitance of an AGC loop as the number of gain stages increase.

To achieve the advantages and in accordance with a purpose of the present invention, as embodied and broadly described, the structure of the invention includes a plurality of gain stages connected in series, that receive and amplify an input RF signal; and a plurality of feedback loops, wherein each feedback loop corresponds to respective ones of the gain stages, and is connected to an input port and output port of the respective gain stage, to filter an offset voltage.

To achieve the advantages and in accordance with a purpose of the present invention, as embodied and broadly described, the invention includes a method for controlling a gain of a signal that includes amplifying the voltage of a signal by propagating the signal through a plurality of gain stages connected in series, wherein each gain stage increases the voltage of the signal, and includes an input port receiving the signal and an output port transmitting the resulting amplified signal and canceling an undesired offset of the resulting amplified signal with a plurality of feedback loops, wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset of its corresponding gain stage.

To achieve the advantages and in accordance with a purpose of the present invention, as embodied and broadly described, the invention includes a direct conversion receiver that includes an amplification unit that receives and amplifies a signal, wherein

the amplification unit includes a plurality of gain stages connected in series to amplify the signal having a voltage, wherein each gain stage increases the voltage of the signal, and includes an input port that receives the signal and an output port that transmits the resulting amplified signal and a plurality of feedback loops that cancel an undesired offset of the resulting amplified signal, wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset of its corresponding gain stage and a mixer that demodulates the amplified signal by mixing the amplified signal with a local oscillation signal to form a demodulated baseband signal.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following, or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

The invention will be described in detail with reference to the following drawings, in which like reference numerals refer to like elements, and wherein:

Figure 1 is a block diagram of a direct conversion receiver according to the related art;



Figure 2a is a block diagram of a DC offset cancelling circuit with a single feedback loop according to the related art;

Figure 2b is a schematic diagram of the DC offset cancelling circuit of Figure 2a;

Figure 3a is a block diagram of a DC offset cancelling circuit with a single feedback loop according to a preferred embodiment of the present invention; and

Figure 3b is a schematic diagram of the DC offset cancelling circuit of Figure 3a.

### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 3a is a block level diagram of a DC offset cancelling circuit 200 in accordance with a preferred embodiment of the present invention. Figure 3b is a schematic diagram of the DC offset cancelling circuit 200 of Fig. 3a. As shown in Figs. 3a and 3b, the DC offset cancelling circuit 200 includes a plurality of gain stages 210 connected in series. However, instead of a single servo feedback loop, each gain stage 210 has its own servo feedback loop and DC offset cancelling circuit 220 to reject the DC offset of the respective gain stage 210. In other preferred embodiments, each gain stage 210 includes a variable gain amplifier (VGA) and each DC offset cancelling circuit 220 includes a high pass filter.

An incoming signal having a voltage  $V_{in}$  is amplified at each gain stage 210. Each individual gain stage 210 ( $i$ ) has a gain of  $A_{vi}$  and the total AGC loop gain is shown at equation 3 as:

$$A_v = \prod_i A_{vi} \quad (3)$$

5 The transfer function for each gain stage 210 is:

$$\frac{sA_{vi}}{s + \frac{g_{mi} A_{vi} A_{vi,DC}}{C_i}}$$

Since the gain stages 210 are cascaded, the overall transfer function for the AGC loop 200, having a number of gain stages 210 ( $N$ ), is shown at equation 4 as:

$$\frac{V_o}{V_{in}} = \left[ \frac{sA_{vi}}{s + \frac{g_{mi} A_{vi} A_{vi,DC}}{C_i}} \right]^N \quad (4)$$

The cut-off frequency  $f_{ci}$  of each gain stage is shown at equation 5 as:

$$f_{ci} = \frac{g_{mi} A_{vi} A_{vi,DC}}{2\pi C_i} \quad (5)$$

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and is preferably substantially equal for best overall performance. The total capacitance value of the AGC according to this preferred embodiment is the sum of the capacitance  $C_i$  for each of the number of gain stages  $N$ . The ratio of total capacitance values indicates the capacitance value required for the DC offset cancellation circuit of the preferred embodiment. This ratio is shown at equation 6 as:

$$\frac{C_r}{\sum_i C_{mi}} = \frac{A_{v,r}}{NA_{v,m}} = \frac{A_{v,m}^{N-1}}{N} \quad (6)$$

where  $C_r$  represents the capacitance value for the related art DC offset cancelling circuit, and  $C_m$  represents the capacitance value for the preferred embodiment of the present invention with multiple DC offset cancelling loops 220. According to the above equation (6), the numerator grows exponentially, but the denominator grows linearly as the number  $N$  of gain stages 210 increases. Thus, the total capacitance value decreases exponentially as the number  $N$  of gain stages 210 increases. Therefore, the capacitance value of the preferred embodiment of the present invention is smaller than the capacitance value of the related art circuit, by several order of magnitudes for only a moderate number of gain stages.

Another advantage of the preferred embodiment of the present invention is that the amount of DC offset rejection is larger in the preferred embodiment than in the related art single servo feedback approach. Based on equation (4), the DC offset decreases

20dB/decade for each gain stage 220, in contrast with 20dB/decade for all the gain stages of the entire related art single feedback loop. In other words, the amount of DC offset is about N times greater in this preferred embodiment of the present invention than in the related art approach. This provides the benefit of substantially eliminating the trade-off between the cut-off frequency and amount of DC offset rejection. The large roll-off rate of the preferred embodiments of the present invention enable the sufficient suppression of DC offset even in the case of low cut-off frequency.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.